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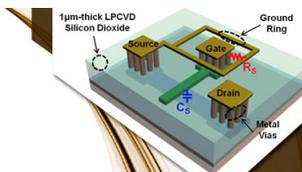
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Thermal boundary conductance response to a change in Cr/Si interfacial properties

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With continued size reduction in microelectronic devices, the boundary conductance between two materials becomes the main channel for thermal dissipation. While many efforts have been directed in studying this interfacial transport, these works have focused on the materials forming the boundary, not the boundary itself. This study focuses on the dependence of thermal boundary conductance on the properties of the region at the Cr/Si interface. The interfacial region of the Cr/Si samples is characterized with Auger electron spectroscopy depth profiling and the boundary conductance is measured with a pump-probe technique. Changes in interfacial properties are shown to significantly affect conductance. © 2006 American Institute of Physics.

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Recent advances in synthesis and design are enabling microelectronic device engineers to maintain Moore's law by providing routine production of well characterized materials with characteristic length scales of tens of nanometers.¹ This decrease in size while maintaining performance and reliability has given rise to the issue of thermal management. For example, metal-semiconductor field effect transistors (MESFETs) are commonly used in microelectronic applications such as microwave devices, logic circuits, and signal processing chips.² The trend towards faster devices creates a voltage modulation that can lead to increased device temperatures. To maintain the MESFET device performance, the generated thermal energy must be dissipated away from the active region. In devices with standard length scales, this thermal dissipation can be predicted by the thermal properties of the materials in the device. However, as length scales continue to decrease the heat dissipation will be contingent on the thermal properties of the underlying packaging and the conductance across the device/packaging boundary must be considered. This thermal boundary conductance (h_{BD}) is also a controlling factor for thermal management in thermoelectrics,^{3,4} thin-film high temperature superconductors,^{5,6} vertical cavity surface emitting lasers,⁷ and optical data storage media.⁸

Not only can the properties of the materials on either side of the interface significantly affect h_{BD} ^{9,10} but simulations have shown that h_{BD} is also affected by the physical properties of the boundary region, such as disorder and intermixing between the two materials.^{11,12} This boundary region must be taken into account as device sizes decrease and pronounced interdiffusion occurs on the order of the characteristic length of the device.¹³

In this letter, the thermal boundary conductance is measured across the Cr/Si interface on two samples with different interfacial properties. The two 50 nm Cr/Si samples were prepared in a multisource, high vacuum thin film sputter deposition system manufactured by the Kurt J. Lesker Company. Both substrates were spin cleaned before being

introduced into the sputtering chamber. One Cr film was deposited on a Si substrate as received while the other Si substrate was backsputter etched at 100 W and 52.5 SCCM (SCCM denotes cubic centimeter per minute at STP) Ar for 5 min to remove some of the native SiO₂. The removal of this oxide layer was performed to reduce Cr–SiO₂ bonding, which impedes diffusion of the Cr into the Si.¹⁴ The roughening of the substrate resulting from the backsputter etching also facilitates Cr/Si diffusion.¹⁵

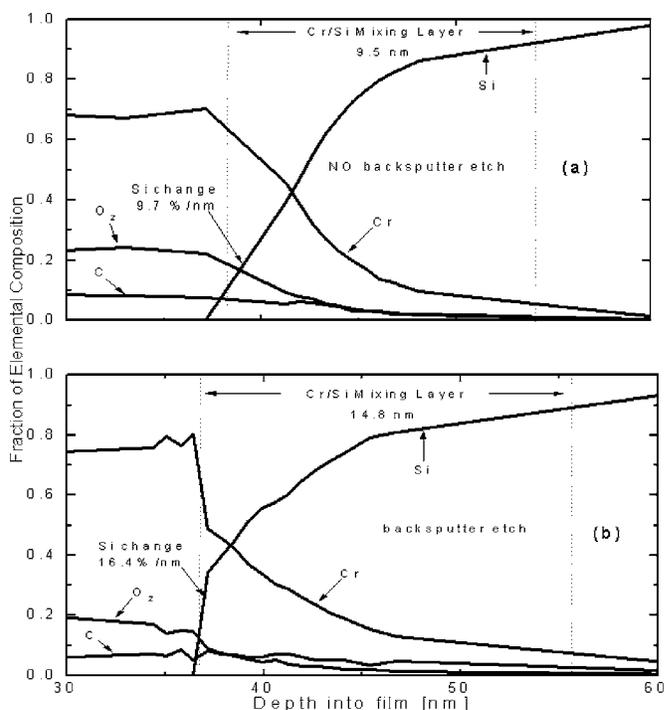


FIG. 1. AES profiles of Cr/Si systems. Top: (a) 50 nm Cr was deposited onto a Si substrate that was not etched. The gradient of the Cr/Si interdiffusion is approximately linear through the ~ 10 nm mixing layer. Bottom: (b) Si substrate was backsputtered for 5 min at 100 W before 50 nm Cr was deposited. The gradient of the Cr/Si interdiffusion is very steep at the beginning of the Cr/Si mixing which could be a result of the etching away of the O₂ layer. The continued etching of the substrate could be the cause of the ~ 15 nm mixing layer.

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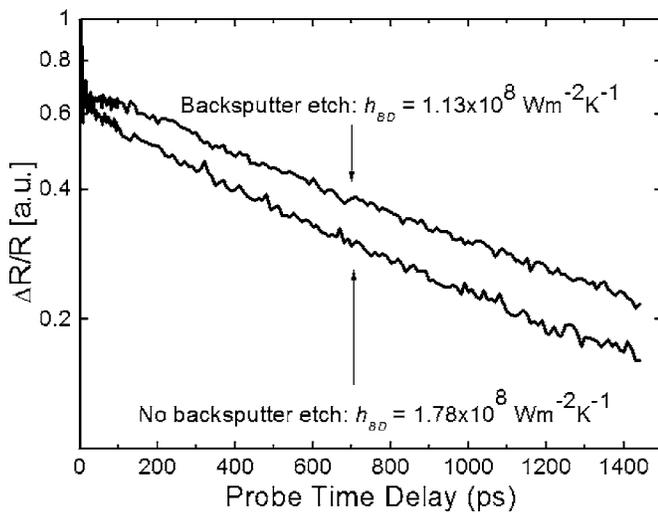


FIG. 2. TTR data of 50 nm Cr/Si. The thermal boundary conductance of the sample that was not prepared by backspattering is about $\sim 60\%$ greater, which could be due to a much less abrupt elemental composition change near the interface or a larger volume of significant Cr/Si mixing as compared to the sample which was backspatter etched.

The elemental composition around the Cr/Si interfaces was characterized by Auger electron spectroscopy (AES) to confirm the variation in mixing layer thickness. Depth profiling was conducted by atomically sputtering away the material with an *in situ* focused Ar ion beam. The AES depth profiles of the two Cr/Si samples are shown in Fig. 1. Figure 1(a) shows the elemental composition profile of Cr deposited on Si with no further substrate preparation other than spin cleaning while Fig. 1(b) gives the elemental composition profile of the Cr/Si system when the Si substrate was backspatter etched. For both depth profiles, only the region around the interface is presented. It should be noted that the vacuum in the sputtering chamber during deposition was $\sim 10^{-6}$ Torr, so the trace amounts of O_2 and C contaminations found in the films are expected. The Cr/Si mixing layer is defined as the region between the points at which Si reaches 10% of the total film composition and Cr reaches 90% of the total film composition. This threshold was chosen since C levels were slightly less than 10% of the total film composition near the interface. It is apparent that backspatter etching the Si substrate prior to deposition causes a significantly more abrupt interface and approximately 5 nm more intermixing of Cr and Si. These phenomena are most likely caused by the reduction of the oxide layer and the physical etching of the Si substrate as a result of Ar ion bombardment during the backspatter. A nearly 50% reduction in O_2 levels was observed at the beginning of the Cr/Si mixing layer as a result of the backspatter etching. This decrease in the oxide layer in the backspattered sample allows for significantly more Cr/Si interdiffusion, and thus a thicker mixing layer.¹⁵

The thermal boundary conductance of these two samples was measured using the pump-probe transient thermoreflectance technique (TTR) with a Coherent Mira 900 oscillator and Rega 9000 amplifier.¹⁶ These data were taken with 10 J/m^2 pump fluence and 1.55 eV probe energy. The data were phase corrected^{17,18} and care was taken to ensure that the probe beam was collimated into the delay stage to avoid misalignment error due to probe beam drift over the duration of the measurement.^{10,17,18} The data were fitted to the thermal model with the details outlined by Stevens *et al.*¹⁰ A best fit

h_{BD} of $1.78 \times 10^8 \text{ W/m}^2 \text{ K}$ was found for the nonbackspattered sample, where the backspattered sample showed a 40% reduction. These measurements were in general agreement with previously reported measurements for h_{BD} across the Cr/Si interface.¹⁰ Comparing these scans with their corresponding AES depth profile, the higher h_{BD} was measured on the sample with the thinner two phase region ($\sim 10 \text{ nm}$ for the nonbackspattered and $\sim 15 \text{ nm}$ for the backspattered). This thinner two phase region also has more uniform mixing as seen in Fig. 1(a) by comparing the rate of change of the Si composition in the first nanometer of the mixing region versus Fig. 2(b). The sample with the thicker two phase region and smaller h_{BD} has a drastic change in elemental composition at the beginning of the boundary region where the large h_{BD} sample shows a more gradual change. Since Cr/Si are well acoustically matched samples¹⁹ in which increased phonon scattering events would decrease h_{BD} ,²⁰ a larger mixing region and more abrupt compositional changes would give rise to more phonon scattering events per area throughout the interface region causing the decrease in the measured h_{BD} .

In conclusion, the thermal boundary conductance across the Cr/Si boundary was measured with the TTR. Two Cr/Si samples were fabricated to produce two different interfacial regions and these regions were characterized by AES depth profiling. The difference in the measured h_{BD} can be attributed in part to the difference between the samples' mixing layer thicknesses and rates of change of Si composition in the two phase regions.

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